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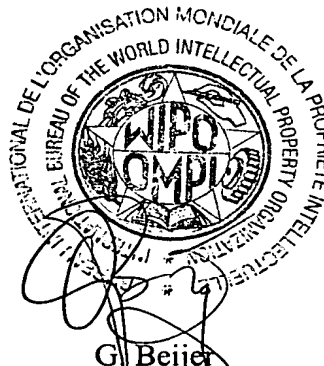
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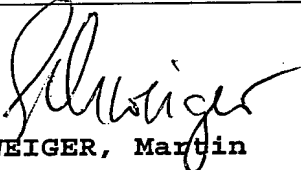
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VIII-1	Declaration as to the identity of the inventor	-	
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VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	-	
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IX	Check list	number of sheets	electronic file(s) attached
IX-1	Request (including declaration sheets)	4	-
IX-2	Description	14	-
IX-3	Claims	4	-
IX-4	Abstract	1	✓
IX-5	Drawings	4	-
IX-7	TOTAL	27	
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IX-8	Fee calculation sheet	✓	-
IX-11	Copy of general power of attorney		-
IX-17	PCT-SAFE physical media	-	✓
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Semiconductor package with perforated substrate

The invention relates to a semiconductor package and to a substrate for a semiconductor package, and to methods for assembling the substrate and semiconductor package.

The performance and reliability of semiconductor packages is limited by stresses within the package which occur during the manufacturing process.

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JP 3283453 discloses a semiconductor package which includes a moisture absorbing material bonded to the rear of the die pad. KR 2002064592-A discloses a semiconductor package which includes a vent hole. These packages are not very reliable and many packages are discarded after manufacturing.

20

It is one object of the invention to provide a more reliable semiconductor package and a simple, cost-effective method for assembling such a package.

This object of the invention is solved by the subject matter of the independent claims. Further improvements arise from the subject matter of the dependent claims.

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A semiconductor package according to the invention comprises a substrate and a semiconductor chip which includes an active surface with a plurality of chip contact areas. The chip contact areas are electrically connected to the upper contact areas of the substrate. The substrate comprises, for example, a redistribution board.

30

The substrate for a semiconductor package according to the invention includes a perforated sheet of core material. The core material comprises an electrically insulating or dielectric material such as a plastic or a ceramic or a BT substrate.

5

The substrate also includes a plurality of upper conducting traces and upper contact pads or areas on its upper surface and a second plurality of lower conductive traces and external contact areas on its bottom surface. A plurality of conducting
10 vias which are positioned essentially vertically through the thickness of the substrate and electrically connect the upper conducting traces and lower conducting traces of the substrate. A plurality of vent holes or non-plated through holes is provided. A layer of solder resist covers the upper and
15 lower surfaces of the substrate leaving the contact areas free from solder resist.

The non-plated through holes or vent holes are positioned essentially vertically in the substrate and penetrate the upper
20 and lower surfaces of the substrate forming open-ended through holes. The vent holes have a diameter of preferably approximately $1\mu\text{m}$ to approximately 5mm or more preferably approximately $10\mu\text{m}$ to approximately 0.5mm or even more preferably approximately $100\mu\text{m}$.

25

The diameters of the through holes have the advantage that the non-plated through holes are positioned laterally between the conducting traces and contact areas on the upper and lower surface of the substrate. The conducting paths are, therefore,
30 not disrupted by the position of the vent holes. Advantageously, the vent holes are included in a standard substrate

which already includes conducting traces and contacts areas in a desired arrangement or design.

Analysis by the inventors has shown that the invention reduces stresses inside the package during the manufacturing process, particularly during the solder reflow process, leading to an improved reliability of the packages. This is the case even when there is moisture inside semiconductor packages.

- 10 The non-plated through holes included in the substrate of the invention have the advantage that moisture escapes from the core material of the substrate through the side walls of the non-plated through holes as the side walls of the vent holes include no metal or electrically conducting coating or layer.
- 15 The metal electro-plated coating on the inner walls of the conducting vias is impermeable to moisture. The metal coating of the conducting vias therefore prevents moisture from escaping from the core material through the centre of the via. The inclusion of the non-plated through holes in the substrate of
- 20 the invention is, therefore, extremely advantageous as moisture escapes from the package in a three-dimensional way.

The substrate according to the invention is advantageously used in a semiconductor package, such as a laminate package

25 which includes a substrate, for example, flip-chip or ball grid array packages. Preferably, the chip is mounted to the substrate by the flip chip technique. Microscopic solder balls connect the chip contact areas to the upper contact areas of the substrate. Preferably the area between the active surface

30 of the chip and the upper surface of the substrate is underfilled by epoxy resin or underfill material. This has the ad-

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vantage that the delicate electrical connections formed by the microscopic solder balls are protected.

5 In an alternative embodiment, the chip is encapsulated by mold material. This has the advantage of protecting the outer surface of the chip and upper surface of the package.

10 The plurality of vent holes are advantageously laterally located towards the centre of the substrate. This advantageously enables moisture in the core material at the centre of the substrate to escape through the vent holes. As the vent holes are positioned in the substrate under the chip and underfill material, the vent holes act as a channel for moisture relief from the underfill material and chip and from the interfaces
15 between the chip, underfill material and substrate. The vent holes provide an efficient moisture relief path, reducing stress at the interfaces and package reliability is improved.

20 Alternatively, the plurality of vent holes are laterally located towards the centre and towards the outer edges of the substrate. This arrangement of the vent holes is particularly advantageous if the chip is overmolded or encapsulated by, for example, mold material or plastic as moisture escapes from the mold material through the vent holes as well as from the outer
25 surfaces. The escape of moisture from the package is therefore enhanced.

30 In one embodiment of the invention the non-plated through holes or vent holes include solder resist. Alternatively, the vent holes are filled by solder resist. This has the advantage that moisture more easily escapes from the package as solder resist is extremely permeable to moisture.

In an embodiment of the invention the vent holes are closed at one end by a layer of solder resist on the upper surface of the substrate. This has the advantage that the solder resist layer is more easily applied to the substrate.

The arrangements of the solder resist have the advantage that underfill material or mold material does not enter the vent holes. As mold material is not permeable to moisture, this has the advantage that the vent holes are not filled or partially filled by moisture blocking material and moisture can more easily escape from the package through the vent holes.

A method to assemble a substrate for a semiconductor package comprises the following steps. Firstly a substrate is provided. The substrate comprises a sheet of core material, a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias connecting the upper conducting traces and lower conducting traces. A plurality of vent holes is then formed in the substrate.

The upper and lower surfaces of the substrate are covered by a layer of solder resist leaving the upper and lower contact areas free from solder resist.

Alternatively, the vent holes are formed in the core material before a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and conducting vias are deposited.

Preferably, the vent holes are formed by drilling.

5 A method to assemble a semiconductor package comprises the following steps. A semiconductor chip comprising an active surface including a plurality of chip contact areas and a substrate as described above is provided.

10 The chip is mounted on the upper surface of a substrate according to the invention by microscopic solder balls between the chip contacts and upper contact areas. A solder reflow is performed. The area between the chip and the upper surface of the substrate is underfilled with epoxy resin and external contacts such as solder balls are attached to the external
15 contact areas of the substrate.

In an embodiment the upper surface of the chip and substrate are covered with mold material to encapsulate the chip.

20 It is an object of the invention to improve the performance and reliability of semiconductor or IC packages. The non-plated through holes or vent holes provided in the substrate provide paths or channels for the free and easy emission of moisture from the package. This is particularly advantageous
25 during the solder reflow process when the package is heated.

The size and distribution of the non-plated through holes within the substrate are chosen so that the channels and surfaces formed by the holes provide an efficient moisture relief
30 from the package in a three-dimensional way.

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Semiconductor packages containing the perforated substrate according to the invention do not suffer high vapour pressure and high moisture content in the interface between the semiconductor chip or die and the die attach or underfill material, the interface between the die attach or underfill material and the substrate, the interface between the mold material or molding compound or plastic housing and the substrate and more advantageously within the substrate. Hygroscopic stresses are reduced by use of the substrate according to the invention and the reliability of the packages is improved. Stresses within and warping of packages which include a perforated substrate according to the invention are reduced and the performance and reliability improved.

15 An embodiment of the invention will now be described by way of example with reference to the drawings.

Figure 1 shows a flip-chip semiconductor package including an exposed semiconductor chip,

20 Figure 2 shows a cross-sectional view of a flip-chip semiconductor package including an overmolded semiconductor chip,

Figure 3 shows a top view of the upper surface of the substrate of the semiconductor package of Figure 1 or Figure 2, and

25 Figure 4 shows a cross-sectional view of an alternative embodiment of a flip-chip package.

Figure 1 shows a cross-sectional view of a semiconductor package 1 which includes an exposed semiconductor chip 2 mounted by the flip-chip technique to a redistribution board 3.

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The redistribution board 3 comprises a sheet of core material 5 and includes a plurality of upper conducting traces 6 and upper contact pads 7 on its upper surface and a second plurality of lower conductive traces 8 and external contact areas 9 on its bottom surface.

The redistribution board 3 also includes a plurality of essentially vertical plated via holes or conducting vias 10 which penetrate the redistribution board from the upper to lower surface. The inner surfaces of the plated via holes 10 are covered by an electrically conducting coating 11 deposited by an electro-plating technique. The upper contact pads 7 on the upper surface of the redistribution board 3 are electrically connected with an external contact area 9 on the bottom surface of the redistribution board 3 by a continuous conducting path formed by upper conductive traces 6, the conducting coating 11 of via holes 10 and the second lower conductive traces 8. A complete conducting path is not seen for every upper contact pad 7 or external contact area 9 in the cross-section of Figure 1 due to the lateral positioning of the upper contact pads 7, external contact areas 9 and conductive traces 6 and 8. The lateral positioning of the upper conducting traces 6 and upper contact pads 7 can be more clearly seen in the top view of Figure 3 which is described later.

25

The redistribution board 3 also includes a plurality of non-plated through holes or vent holes 4 which are positioned essentially vertically and penetrate the redistribution board from the upper to the lower surface. The inner surface of the non-plated through holes 4 does not include a metal coating. The non-plated through holes 4 are laterally positioned in the redistribution board 3 in areas which do not include conduc-

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tive traces or contact areas on either the upper or lower surface. The non-plated through holes 4 and plated via holes 10 are located laterally throughout the redistribution board 3; Some are positioned in the redistribution board 3 towards the lateral centre so that they are under the chip 2 and others are positioned towards the outer edges of the redistribution board 3 so that they are laterally adjacent to the chip 2.

Solder balls 12 are attached to the external contact areas 9 to provide the electrical connection from the package 1 to an external circuit board (which is not shown in the Figure).

The semiconductor chip 2 comprises an active surface including a plurality of chip contact areas 13 and a passive surface. The chip 2 is electrically connected to the redistribution board 3 by microscopic solder balls 14 between the chip contact areas 13 and the upper contact pads 7 on the upper surface of the redistribution board 3.

The upper and lower surfaces of the redistribution board are coated with a layer of solder resist 15. The volume of the plated via holes 10 and non-plated through holes 4 is also filled by the solder resist layer 15. The contact pads 7, contact areas 8 and solder balls 14 are not covered by the solder resist layer 15. The area between the active surface of the chip 2 and the upper surface of the redistribution board 3 is filled by underfill material 16.

The different paths by which moisture can exit the package to the environment are indicated by the arrows 17. Moisture exits the chip 2 and epoxy underfill 16 mainly downwards through the solder resist 15 located in the non-plated through holes 4 as

well as through the plated via holes 10 and from the outer surfaces of the chip 2 and epoxy underfill 6 which are in contact with the environment.

5 Moisture contained within the core material 5 of the redistribution board 3 exits mainly through the side walls of the non-plated through holes 4 and the solder resist within them. For non-plated through holes 4 located under the semiconductor chip 2, the moisture exits mainly downwards. Moisture within
10 the core material 5 also exits the redistribution board 3 from its outer surfaces.

Figure 2 shows a cross-sectional view of an embodiment of the invention which includes a flip-chip semiconductor package 18
15 including a semiconductor chip 2 which is encapsulated by mold material 19. The redistribution board of the package 18 is essentially the same as that of package 1 shown in Figure 1. Parts of the package which are similar have the same reference number and are not necessarily described again. The chip 2 and
20 upper surface of the redistribution board 3 are covered by mold material 19. As indicated by the arrows 17, moisture exits the mold material 19 mainly through the solder resist within the via holes 10 and non-plated through holes 4 as well as through the outer surfaces of the mold material 19 which
25 are in contact with the environment.

Figure 3 shows a plan view of the upper surface of the redistribution board 3 of the semiconductor package 1, 18 of Figure 1 or Figure 2. Contact pads 7 are connected by conductive
30 traces 6 to plated via holes 10. The redistribution board 3 also includes a plurality of non-plated through holes 4 which are laterally located in the redistribution board 3 between

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the conductive traces 6, contact pads 7 and plated via holes 10. Some of the non-plated through holes 4 are located towards the centre of the redistribution board 3 while others are located towards the outer edges of the redistribution board 3.

5

Figure 4 shows a cross-sectional view of a flip-chip semiconductor package 20 including a semiconductor chip 2 according to a further embodiment of the invention. The redistribution board of the package 20 is similar to that of package 1 and 18 shown in Figures 1 and 2. Parts of the package which are similar have the same reference number and are not described again. In this embodiment of the invention, the redistribution board 21 includes non-plated through holes or vent holes 22 which are closed at the upper surface of the redistribution board 21 by a layer of solder resist 15. The vent holes 22 are not filled by solder resist.

15

The invention also relates to methods to assemble a substrate and a semiconductor package.

20

In the first step of the process, a redistribution board 3; 21 is provided. The redistribution board 3; 21 comprises a sheet of insulating core material 5 and a plurality of contact traces 6 and contact pads 7 on its upper surface, a second plurality of conducting traces 8 and external contact areas 9 on its bottom surface and conducting vias or plated via holes 10 connecting conducting traces 6 and lower conducting traces 8. A plurality of vent holes 4 are then drilled through the redistribution board 3, forming through-holes from the upper to the lower surface. The upper and lower surfaces of the redistribution board 3; 21 are then covered by a layer of solder

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resist 15 leaving the contact areas 6 and 8 free from solder resist 15.

In one embodiment of the invention the vent holes 4 are filled with solder resist 15. In an alternative embodiment, the vent holes 22 are closed at the upper surface of the redistribution board by solder resist 15.

The redistribution board 3; 21 assembled using one of the above method is then used assemble a semiconductor package 1; 18; 20. A semiconductor chip 2 comprising an active surface including a plurality of chip contact areas 13 is mounted on the upper surface of the redistribution board 3; 21 by microscopic solder balls 14 between the chip contacts 13 and upper contact pads 7.

The package 1 then undergoes a solder reflow heat treatment. The area between the chip 2 and the upper surface of the redistribution board 3; 21 is underfilled by epoxy resin or underfill material 16. Solder balls 12 are attached to the external contacts 9 of the redistribution board 3; 21.

In an alternative embodiment of the method, after the semiconductor chip 2 is underfilled with underfill material 16, the upper surface of the chip 2 and redistribution board 3 are coated by mold material 19 to form an over-molded semiconductor package 18.

In an alternative method, the vent holes 4; 22 are drilled into the core material 5 of the redistribution board 3; 21 before the conductive traces 6 and 8, contact areas 7 and 9 and

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conducting vias 10 are deposited on the redistribution board
3; 21.

The semiconductor packages 1; 18; 20 are then tested, packaged
5 and transported to the customer. The semiconductor packages
are mounted to external substrates such as a printed circuit
board.

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18

Reference Numbers

- 1 semiconductor package
- 5 2 semiconductor chip
- 3 redistribution board
- 4 non-plated through hole
- 5 core material
- 6 upper conductive trace
- 10 7 upper contact pad
- 8 lower conductive trace
- 9 external contact area
- 10 plated via hole
- 11 metal coating
- 15 12 solder ball
- 13 chip contact area
- 14 microscopic solder ball
- 15 solder resist
- 16 underfill material
- 20 17 arrow
- 18 overmolded semiconductor package
- 19 mold material
- 20 semiconductor package
- 21 redistribution board
- 25 22 closed-end vent holes

Patent claims

1. A method to assemble a substrate (3; 21) for a semiconductor package (1, 18) comprising the following steps:
 - 5 - providing a substrate (3; 21) comprising a sheet of core material (5) and a plurality of upper contact traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conducting traces (8) and external contact areas (9) on its bottom surface
 - 10 and conducting vias (10) connecting the upper conducting traces (6) and lower conducting traces (8),
 - forming a plurality of vent holes (4) in the substrate (3), and
 - covering the upper and lower surfaces of the substrate
 - 15 (3; 21) by a layer of solder resist (15) leaving the contact areas (6 and 8) free from solder resist (15).
2. A method to assemble a substrate (21) according to claim 1 characterized in that
- 20 the vent holes (22) are closed at one end by a layer of solder resist (15) on the upper surface of the substrate (21).
3. A method to assemble a substrate (3) according to claim 1 or claim 2
- 25 characterized in that the vent holes (4) are include solder resist (15).
4. A method to assemble a substrate (3; 21) according to one
- 30 of claims 1 to 3 characterized in that the vent holes (4, 22) are formed by drilling.

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5. A method to assemble a substrate (3; 21) of one of claims 1 to 4

characterized in that

5 the vent holes (4) are formed in the core material (5) before a plurality of upper contact traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conducting traces (8) and external contact areas (9) on its bottom surface and conducting vias (10) are deposited.

6. A method to assemble a semiconductor package (1; 18; 20), comprising the following steps:

- 15 - providing the substrate (3; 21) with a method according to one of claims 1 to 5,
- providing a semiconductor chip (2) comprising an active surface including a plurality of chip contact areas (13),
- 20 - mounting the chip (2) on the upper surface of the redistribution board (3; 21) by microscopic solder balls (14) between the chip contacts (13) and upper contact areas (7),
- performing a solder reflow,
- 25 - underfilling the area between the chip (2) and the upper surface of the redistribution board (3; 21) with epoxy resin (16).

7. A method to assemble a semiconductor package (18) characterized in that

30 the upper surface of the chip (2) and substrate (3; 21) are covered with mold material (19).

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8. A substrate (3; 21) for a semiconductor package (1; 18; 20) comprising:

- a sheet of core material (5),
- a plurality of upper conducting traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conductive traces (8) and external contact areas (9) on its bottom surface and a plurality of conducting vias (10) connecting the upper conducting traces (6) and lower conducting traces (8),
- a plurality of vent holes (4), and
- a layer of solder resist (15) covering the upper and lower surfaces of the substrate (3) leaving the contact areas (6 and 8) free from solder resist (15).

9. A substrate (3) according to claim 8 characterized in that the vent holes (4) are include solder resist (15).

10. A substrate (21) according to claim 8 characterized in that the vent holes (22) are closed at one end by a layer of solder resist (15) on the upper surface of the substrate (21).

11. A substrate (3; 21) according to one of claims 8 to 10 characterized in that the plurality of vent holes (4; 22) are laterally located towards the centre of the substrate (3; 21).

12. A substrate (3, 21) according to one of claims 8 to 11 characterized in that

the plurality of vent holes (4; 22) are laterally located towards the centre and towards the outer edges of the substrate (3, 21).

- 5 13.A substrate (3; 21) according to one of claims 8 to 12 characterized in that
the vent holes (4; 22) have a diameter of approximately 1µm to approximately 5mm or approximately 10µm to approximately 0.5mm or approximately 100µm.

10

- 14.A semiconductor package (1; 18; 20) comprising:
- a substrate (3; 21) according to one of claims 8 to 13,
- a semiconductor chip (2) including an active surface with a plurality of chip contact areas (13), electrically connected to the substrate (3; 21).

15

- 15.A semiconductor package (18; 20) according to claim 14 characterized in that
the chip (2) is encapsulated by mold material (19).

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- 16.A semiconductor package (1; 18; 20) according to claim 14 or claim 15 characterized in that
the chip (2) is mounted to the substrate (3; 21) by the flip-chip technique.

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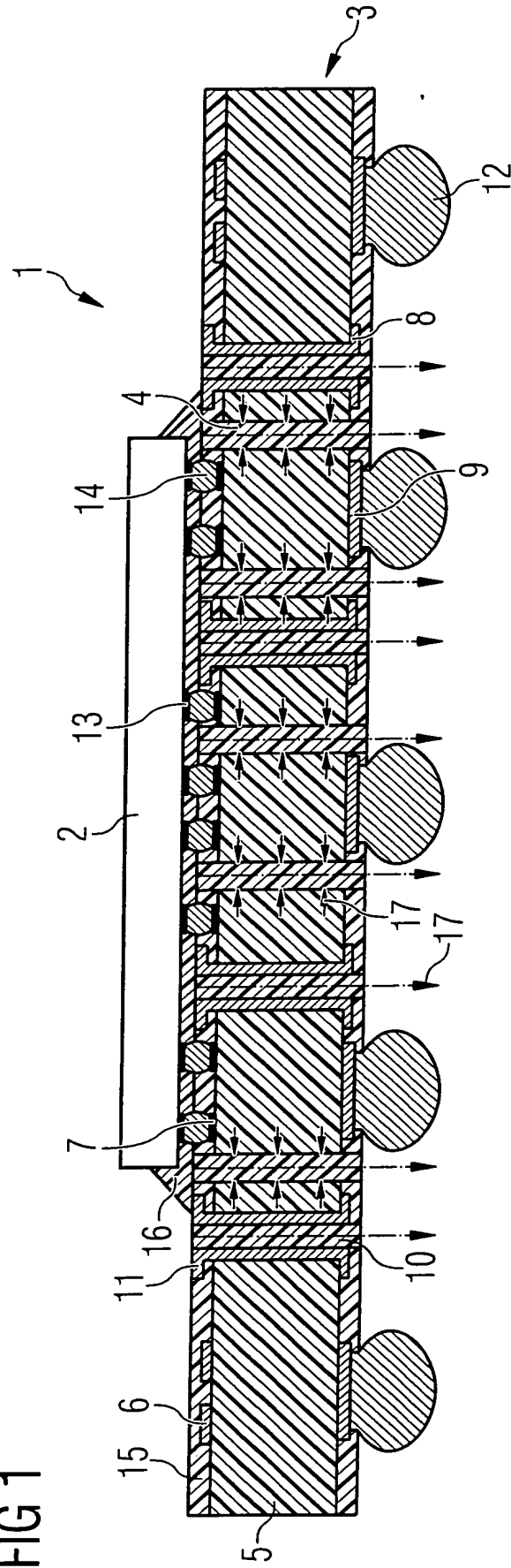
Abstract

A semiconductor package (1; 18; 20) comprises a substrate (3; 21) and a semiconductor chip (2) which includes an active surface with a plurality of chip contact areas (13). The chip (2) is electrically connected to the substrate (3; 21). The substrate comprises a sheet of core material (5), a plurality of upper conducting traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conductive traces (8) and external contact areas (9) on its bottom surface. A plurality of conducting vias (10) connect the conducting traces (6) and lower conducting traces (8). The substrate (3; 21) also includes a plurality of vent holes (4; 22) and a layer of solder resist (15) covering the upper and lower surfaces of the substrate (3) leaving the contact areas (6 and 8) free from solder resist (15).

20 [Fig. 1]

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FIG 1



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FIG 2

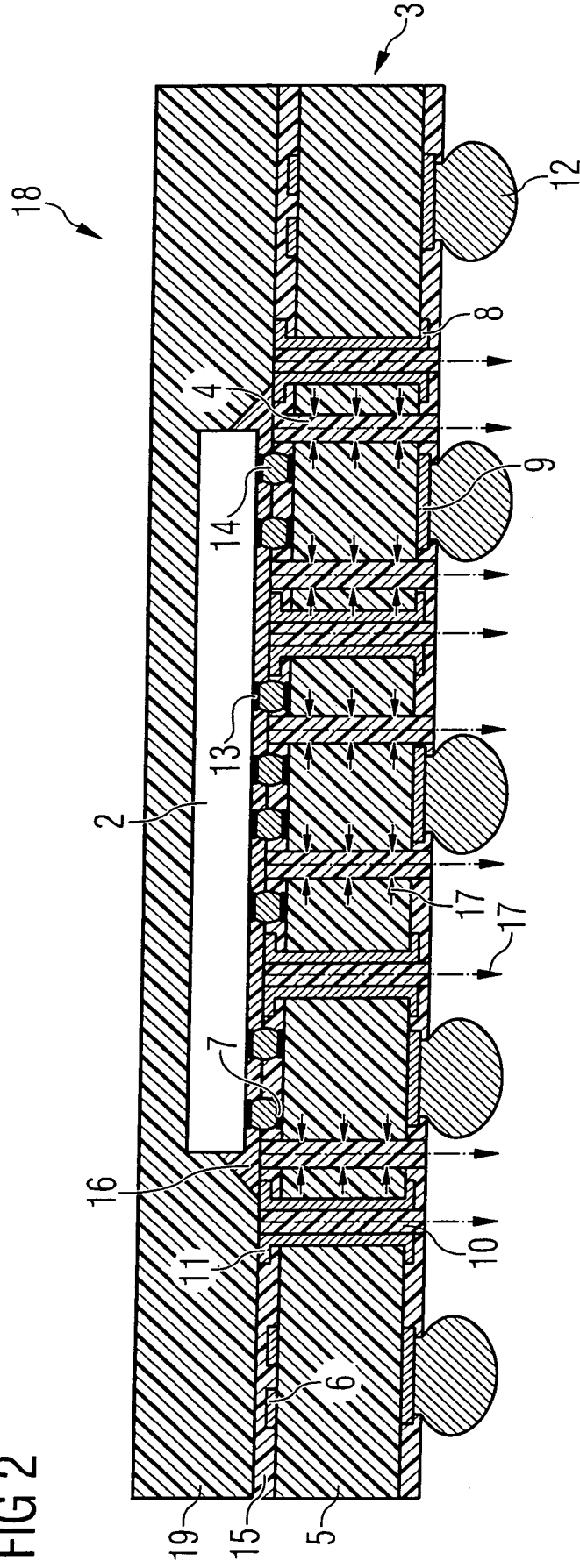
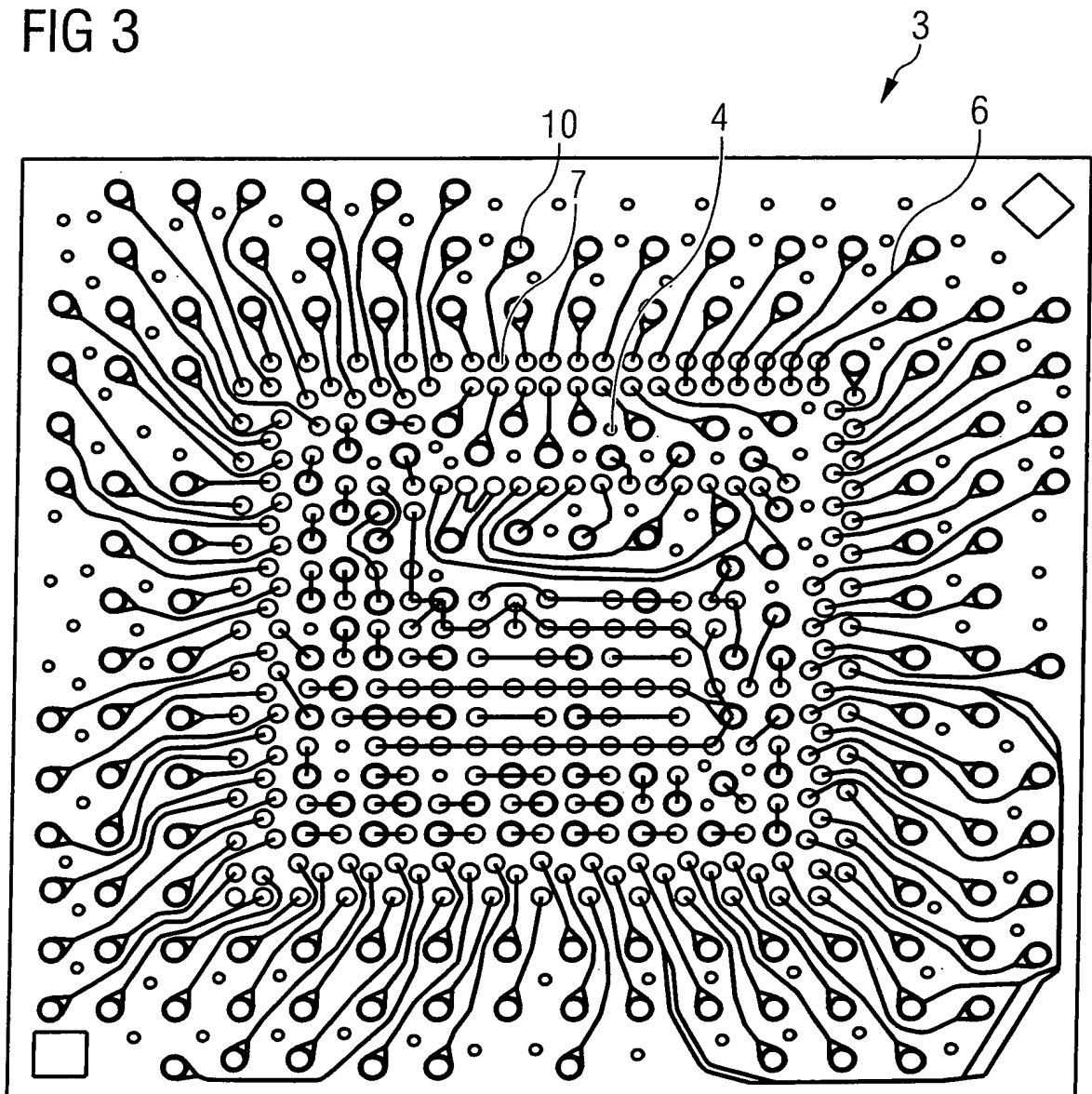


FIG 3



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FIG 4

